A Set of Integrated Circuits for 60 GHz Radio Front-End

Mikko Kärkkäinen[1], Mikko Varonen[1], Jan Riska[1], Pekka Kangaslahti[1,2] and Veikko Porra[1]

[1]Electronic Circuit Design Laboratory, Helsinki University of Technology, Espoo, P.O. Box 3000, FIN-02015 HUT, Finland [2]Ylinen Electronics, Teollisuustie 9A, FIN-02700 Kauniainen, Finland

***Abstract* — This paper describes results obtained within the MMIC research activity at the Helsinki University of Technology (HUT). These MMICs were developed for a 60 GHz broadband radio front-end. A set of circuits is reported including power, low noise amplifiers, mixers and signal generation circuits. They have been fabricated with a commercially available 0.15 μm GaAs pseudomorphic HEMT technology. Finally, the performance of the circuits was measured at 60 GHz frequency: The power amplifier has 14 dBm output compression point and 15.5 dB small signal gain. The low noise amplifier exhibits 24 dB of gain with 3.5 dB noise figure and the up-conversion mixer circuit has 12.7 dB of conversion loss.**

I. INTRODUCTION

The MMIC radio front end is intended for applications such as a wireless local area network (WLAN), which can offer more capacity at millimeter wave frequencies due to wider absolute bandwidth. The high data rates of emerging wireless broadband networks that enable mobile multimedia and improve wireless data access speeds need more bandwidth and it is easily available at the 60 GHz frequency range. The drawback is the more complex and expensive techniques needed to design MMICs. The focus of wireless broadband networks in Europe is on 5 (HIPERLAN), 17 (HIPERLAN), 40 (MBS) and 60 GHz (WLAN and MBS). The 60 GHz range is available for wireless broadband networks in Europe, US and Japan [1].

The oxygen molecule resonance causes absorption around the 60 GHz frequency band and makes it suitable for high-density communication networks. The coverage is not as problematic as the interference from short bursts in unstable handover situations and fading due to body shadowing issues. In spite of the challenges, the 60 GHz range seems to be feasible for wireless communication systems in office environment and hot spots in high population areas [2].

Commercially available millimeter wave technologies have become mature enough for integration of 60 GHz radio systems [3]. Here we present a set of 60 GHz monolithic integrated circuits. The second versions of the amplifiers and a mixer together with previously reported 60 GHz MMIC circuits are intended for building a 60 GHz prototype radio front end shown in Fig. 1 [4].

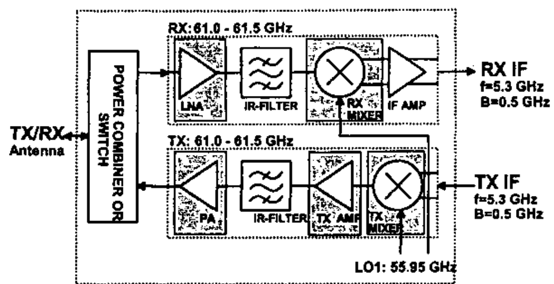


Fig. 1. The block diagram of the proposed 60 GHz radio front end.

II. DESIGN, FABRICATION AND MEASURED RESULTS

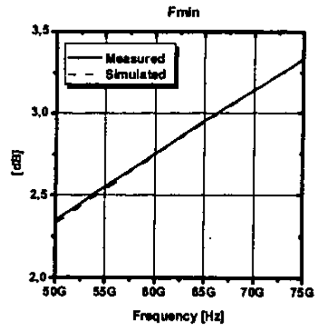
InP-HEMT devices have lower noise figures than GaAs-HEMTs at millimeter waves, but lower cost and easier availability made the pseudomorphic GaAs HEMT processes more suitable for our design goals. The chosen process is commercially available and it features 0.15 μm GaAs PHEMT devices. Passive circuit elements such as ground VIA-holes, substrate resistors and metal-insulator-metal (MIM)-capacitors are offered with this process. The transistor f_t was 100 GHz.

A. Low Noise Amplifier

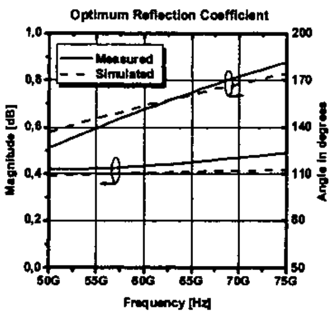
Because no noise model was available from the foundry, a simple model was fitted to simulate transistor's noise parameters from 50 to 75 GHz. A single parameter model has proven adequate to model the transistor's noise characteristics in our case. The measured and simulated noise parameters of a 2x25 mm PHEMT biased at 0.0 V of gate voltage and 14 mA of drain current are presented in figures 2(a-c). Sometimes a two-parameter or even a three-parameter temperature noise model can be used [5]. The physical temperatures of the drain, gate and the gate to source resistances are increased to increase their contribution of noise power in these models. The third parameter is needed if the gate Schottky-contact has a

0-7803-7239-5/02/$10.00 © 2002 IEEE

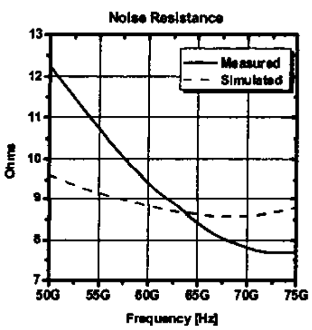
significant leakage current. This type of a noise model was originally presented by Pospieszalski [6].



(a)



(b)



(c)

Fig. 2(a-c). The 2x25μm PHEMT noise characteristics.

Unfortunately, when the first three stage LNA was designed, the noise measurement data was inadequate and we had to rely on inductive series feedback as well as on PHEMT-transistor's low noise properties in order to achieve lower noise level. The size of the PHEMTs was 2x35-μm and the devices are biased at a drain voltage of 2.5 V and a drain current of 14 mA. The chips were matched to 50 Ω and AC-coupled through DC-blocking capacitors at the input and output. A number of precautions were emphasized to avoid any low-frequency instability. Parallel RC-networks in the bias lines were used to avoid oscillations introduced by the power supply. In addition, resistively loaded high-impedance stubs were used for out-of-band stabilization. Finally, large decoupling capacitors were attached to the bias lines to suppress undesired biasing feedback and to further enhance stability.

In figure 5 are the measured noise figure and small signal gain of the LNA. The noise figure at 60 GHz is 4.8 dB and the gain 18 dB. The input return loss is only 6 dB, but on the other hand the output return loss was better than 10 dB from 56 GHz to 64 GHz.

A new version of the LNA was designed and measured. The new 3-stage LNA has two 2x25-μm transistors with a 2x50-μm output stage. The first two stages are biased at 2.5 V / 14 mA and the last stage at 4.5 V / 30 mA (drain voltage/current). The larger last stage is better for linearity and gain. The short circuited bias line and its stabilization RC-network were simplified in order to avoid creating a loop structure. Otherwise, similar stabilization methods were used as in the first LNA.

The new LNA was mounted on a measurement jig and more stabilizing elements were attached to the DC-circuitry. The measured gain is 24 dB and the noise figure is 3.5 dB at 60 GHz. The use of noise model in the design improved the noise figure by 1.5 dB. The measured S21 is compared to the gain obtained from the noise measurement (Figure 6).

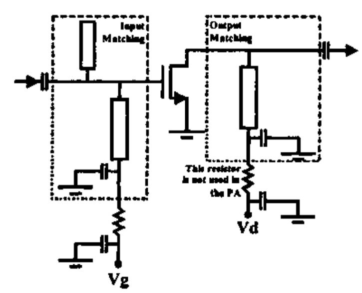


Fig 3. The amplifier design principle.

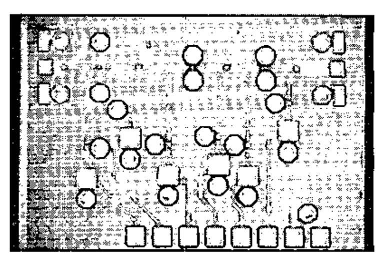


Fig. 4. The microphotograph of the new low noise amplifier. The chip size is 2.0 x 1.5 mm.

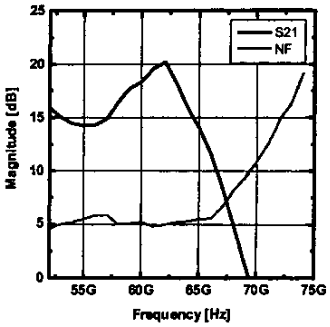


Fig. 5. The measured gain and the noise figure of the previously fabricated LNA.

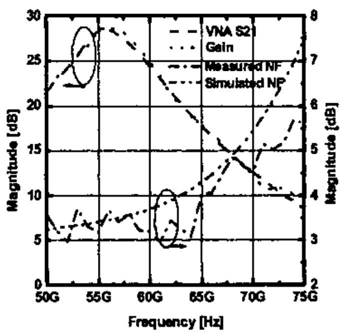


Fig. 6. The measured gain and noise figure of the new LNA.

B. Medium Power Amplifier

The power amplifier designs were chosen to achieve maximum power output, while allowing wide bandwidth. The devices and the power amplifier designs were characterized using the harmonic balance technique.

The first version is a three-stage single-ended amplifier with a total output periphery of 200 µm. Because of being a prototype amplifier the driving stages were designed to have the same size. The amplifier was biased at 3.5 V of drain voltage and 50 mA of drain current per stage. The same precautions to avoid low frequency instability were taken as with the low noise amplifier.

A new version was designed to achieve better gain and still maintain the output power level. The size of the power, the driver and the gain stages were chosen to have peripheries of 210 µm, 140 µm and 70 µm respectively. The amplifier was designed for low drain bias of 3.0 V and a total drain current of 150 mA.

The small signal gain of the prototype version was 12 dB. The input and output return losses were better than 10 dB over a 10 % frequency bandwidth. The 1 dB output power compression point was at 15 dBm level.

The measured scattering parameters of the new power amplifier are shown in figure 7. It achieved 15.5 dB linear gain and the output compression point was about 14 dBm (Fig. 8).

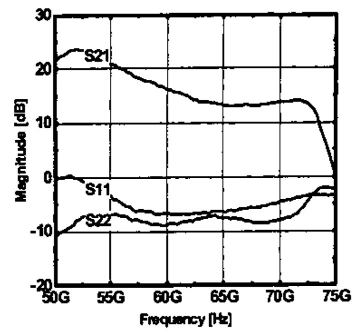


Fig. 7. The measured scattering parameters of the new power amplifier.

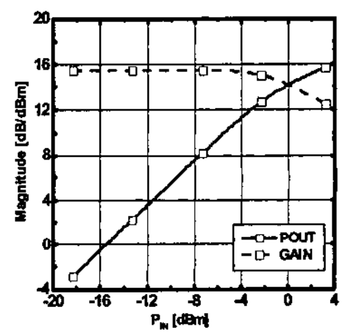


Fig. 8. The measured power sweep of the new power amplifier.

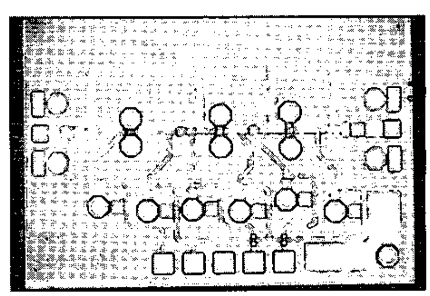


Fig. 9. The microphotograph of the new power amplifier. The chip size is 2.0 x 1.5 mm.

C. Resistive Mixer And Signal Generation Circuits For 60 GHz Frequency Range

A single transistor resistive mixer was designed using 0.25 µm GaAs-PHEMT process. The measured conversion loss is presented in figure 12. The results were obtained in upconversion configuration with local oscillator signal at 56 GHz and intermediate frequency at 4-6 GHz. The IF-port was left unmatched while the RF-port was matched with a short-circuited shunt stub. A conversion loss of 12.7 dB was obtained at 62 GHz output frequency. This is 4 dB higher than the designed loss and the results might be affected by the low LO power level of +2 dBm delivered to the MMIC. The designed level is at +10 dBm.

A single balanced resistive mixer was previously designed using coplanar technology. In addition, we have a frequency doubler for local oscillator signal generation at 60 GHz. These are reported in [4].

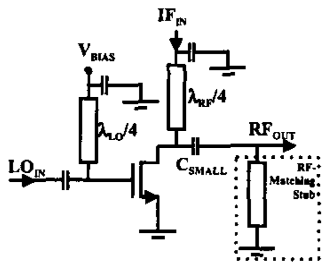


Fig. 10. The mixer circuit.

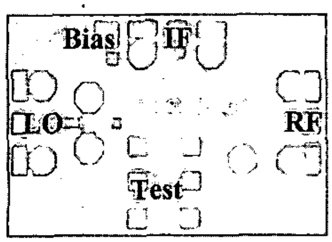


Fig. 11. The microphotograph of the single PHEMT resistive mixer. The chip size is 1.5 x 1.0 mm.

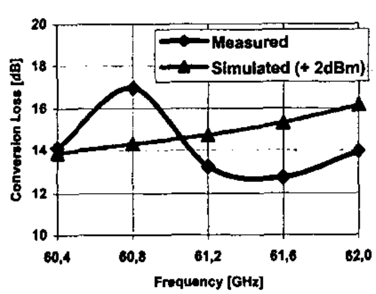


Fig. 12. The measured conversion loss of the mixer.

III. Conclusions

A set of millimeter wave MMICs is reported. They are intended for a 60 GHz broadband radio front end. The performance of the successfully designed and fabricated amplifiers and mixer circuits were reported.

Acknowledgements

This research was supported by the Finnish Technology Development Centre, Nokia Networks, Nokia Research Center and Ylinen Electronics. We are grateful to ESA external laboratory MilliLab for performing the on-chip measurements of transistor noise parameters and LNA noise figures.

References

[1] J. Mikkonen, C. Corrado, C. Evci, M. Prögler, "Emerging Wireless Broadband Networks," *IEEE Communications Magazine*, vol. 36, no. 2, pp. 112-117, Feb. 1998.

[2] A. Bria, F. Gessler, O. Queseth, R. Stridh, M. Unbehaun, J. Wu, J. Zander, M. Flament, "4th-Generation Wireless Infrastructures: Scenarios and Research Challenges", *IEEE Personal Communications*, vol. 8, no. 6, pp. 25-31, Dec. 2001.

[3] P. Mikkonen, "Modern 60 GHz Radio Link," *Proc. of 29th European Microwave Conference*, Munich, vol. 3, pp. 83-86, 1999.

[4] J. Riska, P. Kangaslahti, M. Kärkkäinen, V. Porra, "Amplifiers and Signal Generation Circuits for 60 GHz Wireless Broadband System", *Proc. of the European Microwave Conference*, Paris, Eumc_P3, 2000.

[5] M. Garcia, J. Stenarson, K. Yhland, H. Zirath, I. Angelov, "A New Extraction Method for the Two-Parameter FET Temperature Noise Model", *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no.11, pp. 1679-1685, 1998.

[6] M. W. Pospieszalski, "Modelling of Noise Parameters of MESFETs and MOSFETs and Their Frequency and Temperature Dependence," *IEEE Transactions on Microwave Theory and Techniques*, vol. 37, no. 9, pp. 1340-1350, 1989.